REMARKS

I. Status of Claims

Claims 1-16 and 18-31 are pending.

Claims 1-16 and 18-31 stand rejected.

Claim 17 was cancelled in a prior response.

Claims 1 and 16 are amended herein.

II. Objections to the Specification

The examiner has objected to the specification as failing to provide proper antecedent basis for the claimed subject matter. Applicant, through his attorney, again wishes to thank the examiner for her observations and has amended the claims and the specification to include corrections to the noted antecedent basis issues.

The applicant submits that the reasons for the examiner's objections to the specification have been overcome and can no longer be sustained. Applicant respectfully requests that the objections be withdrawn.

A. Examiner's Objections to Specification per 37 CFR 1.75(d) and MPEP §608.01(o), Regarding Terminal Connections

The examiner has objected to the specification as failing to provide proper antecedent basis for the claimed subject matter. Specifically the examiner states "Claims 1 and 16 recite terminal connections for the first through fourth transistors that are specific to the embodiment shown in Figure 4a; however, dependent claims, such as 3-7 and 19-23, recite limitations that are drawn to Figure 3a."

Response: The terminal connections for Figure 3a and Figure 4a are the same, as stated in specification paragraph 27, second sentence referring to Figure 4a: "In this second embodiment, shown as a NAND gate combinational logic circuit, the configuration is the same as that described with regard to Figure 3a and need not be repeated." The only difference between Figure 3a and Figure 4a is that "In this embodiment, p-type transistors replace the n-type transistors and n-type transistors replace the p-type transistors." (Specification paragraph 27). Further evidence that the terminal connections of Figure 3a and Figure 4a are the same, is evidenced by paragraph 28, sentence 3 referring to Figure 4a: "[S]ource terminals of the p-type transistor 410 and transistor 430 are electrically connected to control line CL_1 145 and CL_2 140 respectively." Similarly Paragraph 21, referring to Figure 3a states: "Source terminals of n-type transistor 310 and transistor 330 are electrically connected to control line CL_1 145 and CL_2 140 respectively."

Thus, the terminal connections in Figure 3a and Figure 4a are the same, only the types of transistors are different in each figure.

B. Examiner's Objections to Specification per 37 CFR 1.75(d) and MPEP §608.01(o), Regarding Power Supply

The examiner has objected to the specification because

> "the present claims also appear to describe structures with the same power supply connected to both the drain and source terminals of the recited transistors. More particularly, Figure 3a depicts the third power supply as being equal to Vdd so, for embodiments corresponding to Figure 3a, the circuit would not operate, seemingly, if the transistors having their drain source path connected to Vdd on one side also had the same path connected to Vdd on the

> other side. Likewise, Figure 4a depicts an embodiment wherein the third power supply is equal to Vss so, similarly, the same problem exists in terms of support for those embodiments reciting source/drain paths of transistors with both ends connected to the same power supplies. The specification does not support such hybrid embodiments nor does it disclose how it would function."

Response: At no time are all transistor drain/source paths connected at both ends to the same voltage. Control lines CL_1 145 and CL_1 140 are typically set in opposite states as described in the specification. See paragraph 21 "In the present invention CL_1 145 and CL_2 140 are set to different voltage levels . . . "; paragraph 22 "control line CL_1 145 is set to a low voltage, Vss, and control line CL_2 is set to a high voltage, Vdd"; paragraph 25 "control line CL_1 145 is set to a high voltage, Vdd, and control line CL_2 140 is set to a low voltage, Vss"; paragraph 29 "in this case, control line CL_1 145 is set to a high voltage, Vdd, and control line CL_2 140 set to a low voltage, Vss"; and paragraph 31 "In this case, control line CL_1 145 is set to a low voltage, Vss, and control line CL_2 140 is set to a high voltage, Vdd." Thus, there is never a case where all transistors have the same voltage applied to both source and drain sides.

Further, the fact that transistor string 410, 425 and 420 (or 310, 325 and 320) might have the same voltage at the extreme ends of the string, does not preclude the transistors from functioning, since not all transistors in the string need to be on to have the proper voltage appear at the output, 122. For example, for the circuit depicted in Figure 4a, when CL_1 145 is at Vss and CL_2 140 is at Vdd (i.e. transistor string 410, 425 and 420 connected at both ends to Vss) , when (n-1)* is high and (n+1)* is high, transistors 420 and 425 are on and the path from Vss to output terminal 122 is complete

from Vss. With the same CL_1, CL_2 voltages when (N-1)* transitions low, the drain of transistor 410 is forced low by the gate/drain capacitance of transistor 410 because that capacitance was previously charged to 5V. That charge is sufficient to force terminal 122 low.

The tables below further explain how the circuits in Figures 3a and 4a function to give the voltage levels shown in figures 3b and 3c and 4b and 4c respectively.

Fig. 3a, Case CL_1 = Vss, CL_2 =Vdd

Transistor	n - 1 = 0 n + 1 =0	n - 1 = 1 n + 1 = 0	n -1 = 0 n + 1 = 1
	Fig. 3b, ¶ 22	Fig. 3b, ¶ 23	Fig. 3b, ¶ 23
320	on	off	on
325	on	on	off
310	off	on	off
330	off	off	off
voltage at 122	Vdd	Vss	Vdd
path to 122	Vdd via FET 320 and FET 325	CL_1 (Vss) via FET 310	Vdd via FET 330 drain forced high by gate/drain capacitance when N+1 goes high

Fig. 3a, Case CL_1 = Vdd, CL_2 = 0

Transistor	n - 1 = 0 n + 1 =0	n - 1 = 1 n + 1 = 0	n -1 = 0 n + 1 = 1
	Fig. 3c, ¶ 25	Fig. 3c	Fig. 3c, ¶26
320	on	off	on
325	on	on	off
310	off	off	off
330	off	off	on
voltage at 122	Vdd	Vdd	Vss
path to 122	Vdd via FET 320 and FET 325	Vdd level by FET 310 drain forced high by gate/drain capacitance when n-1 goes high	CL_2 (Vss) via FET 330

Fig. 4a, Case CL_1 = Vdd, CL_2 =Vss

Transistor	(n – 1)* = 1 (n + 1)* = 1	(n – 1)* = 1 (n + 1)* = 0	(n -1)* = 0 (n + 1)* = 1
	Fig. 4b, ¶ 29	Fig. 4b	Fig. 4b , 30¶
410	off	off	on
425	on	off	on*
420	on	on	off
430	off	off	off
voltage at 122	Vss	Vss	Vdd
path to 122	Vss via FET 420 and FET 425	Vss level by FET 430 source being forced low by gate/source capacitance when (n+1)* goes low	CL_1 (Vdd) via FET 410. Note FET 425 is on because its source is at Vss due to drain of FET 420 being forced low by drain/source capacitance when (n-1)* goes low.

Fig. 4a, Case CL_1 = Vss, CL2 =Vdd

Transistor	(n – 1)* = 1 (n + 1)* = 1	(n – 1)* = 1 (n + 1)* = 0	(n -1)* = 0 (n + 1)* = 1
	Fig. 4c, ¶ 32	Fig. 4c, ¶ 31	Fig. 4c , ¶ 33
410	off	off	off
425	on	off	on*
420	on	on	off
430	off	on	off
voltage at 122	Vss	Vdd	Vss
path to 122	Vss via FET 420 and FET 425	CL_2 (Vdd) via FET 430	Vss level by FET 410 drain being forced low by gate/drain capacitance when (n-1)* goes low. Note, FET 425 is on because its source is at Vss due to drain of FET 420 being forced low by its gate/drain capacitance when (n-1)* goes low.

Finally, the applicant includes here two SPICE circuit simulations to demonstrate that the circuits do function in practice as described in the specification. The first shows the circuit output (node 1) for Figure 3a where CL_1 is high and CL_2 is low, i.e. Figure 3c. The second chart shows the circuit output for Figure 4a where CL_1 is low and CL_2 is high, i.e. Figure 4c.

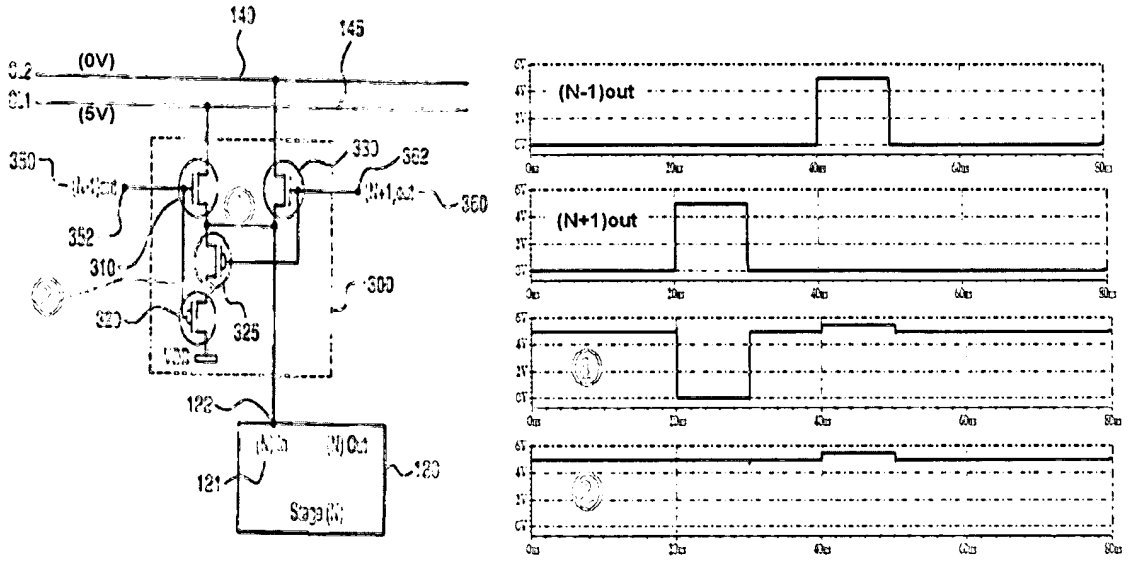

FIG. 3a

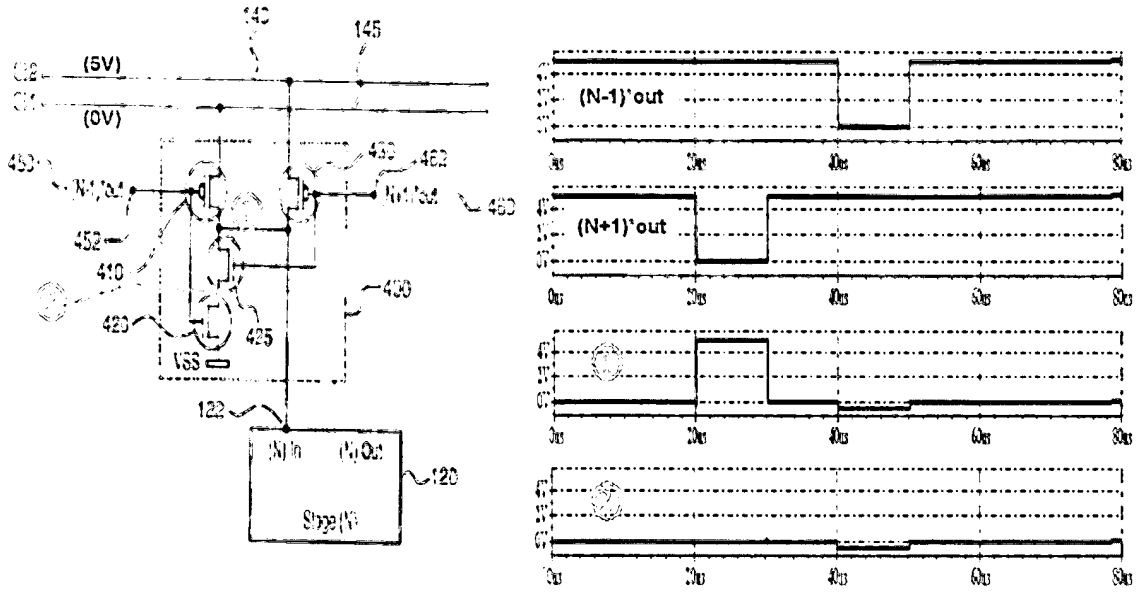

FIG. 4a

III. Objections to the Claims

The examiner has objected to claims 1 and 16 for containing informalities. Applicant, through his attorney, again wishes to thank the examiner for her observations and has made new claims which include corrections to the noted informalities.

Having amended these claims to correct the informalities, applicant submits that the reasons for the examiner's objection to the claims have been overcome and can no longer be sustained. Applicant respectfully requests that the objection be withdrawn.

IV. Rejection of Claims Based on 35 U.S.C. §112

The examiner has rejected claims 1-16 and 18-31 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim

the subject matter which applicant regards as the invention. In particular, the examiner cited as lacking a clear antecedent basis or being claimed repetitively the terms in claims 1 and 16: "a first control line", "the second terminal", "the first transistor", "the drain", "the second transistor", "the source" and "the third transistor."

Having amended these claims to correct these issues, applicant submits that the reasons for the examiner's rejection of the claims have been traversed and can no longer be sustained. Applicant respectfully requests that claims 1-16 and 18-31 be allowed.

CONCLUSION

Having addressed the examiner's rejections, applicant submits that the reasons for the examiner's rejections have been overcome by the amendments to the specification and claims and remarks made herein, and the objections and rejections can no longer be sustained. Applicant respectfully requests reconsideration and withdrawal of the rejections and that a Notice of Allowance be issued.

Should any unresolved issues remain, the examiner is requested to call Applicant's attorney at the telephone number below.

The Commissioner for Patents is hereby authorized to charge any fees or credit any excess payment that may be associated with this communication to Duane Morris LLP deposit account 50-2061.

Respectfully submitted,

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